UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/518,158	12/10/2004	Jean-Michel Reynes	SC0985ET	2901

23125 7590 06/26/2006

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
INGHAM, JOHN C	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/518,158	REYNES ET AL.	
	Examiner	Art Unit	
	John C. Ingham	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *10 December 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/11/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Power Semiconductor Device with a Single Continuous Base Region and Method of Manufacturing the Same.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims **1-13** are rejected under 35 U.S.C. 102(b) as being anticipated by Neilson (US 5,399,892).

4. Regarding claim **1**, Neilson discloses in Fig 4 a power semiconductor device comprising a two-dimensional array of individual cells formed on a semiconductor substrate, each cell having source regions (46) within base regions (50) in the substrate, characterized in that the source regions of the cells of the array comprise a plurality of source region branches (46) each extending radially towards at least one source region branch of an adjacent cell (Fig 10), the source region branches of adjacent cells presenting juxtaposed ends, the base regions (50) of the cells of the array

comprising a corresponding plurality of base region branches extending radially towards at least one base region branch of an adjacent cell (Fig 10), and the base region branches of adjacent cells merging together adjacent and between said juxtaposed ends to form a single and substantially uniformly doped base region surrounding said source regions of the individual cells of said array (Fig 10, col 1 ln 22-30).

5. Regarding claim **2**, Neilson discloses in Fig 4 the device of claim 1, wherein said plurality of radially extending branches (46, Fig 5) of an individual cell intersect at a central enlarged area (Fig 6) having contact cut-out portions whose width is larger than the width of said radially extending branches.

6. Regarding claim **3**, Neilson discloses in Fig 4 the device of claim 2 wherein the cut-out portions (across 6-6) of said enlarged area are straight segments.

7. Regarding claim **4**, Neilson discloses in Fig 4 the device of claim 1 wherein said radially extending branches (46) of each cell are linear, with constant width.

8. Regarding claim **5**, Neilson discloses in Fig 5 the device of claim 1 wherein each individual cell has at least three (four) radially extending branches arranged in such a way that the area defined (52) by the merging branches is a polygon.

9. Regarding claim **6**, Neilson discloses in Fig 10 the device of claim 1 and comprising at least one drain electrode (unlabeled, below item 40) contacting a face of said semiconductor substrate opposite said source regions.

10. Regarding claim **7**, Neilson discloses in Fig 10 the device of claim 1 further comprising physically isolated drain regions (52) in the substrate and wherein said

physically isolated drain regions have a depth equivalent to the depth of said base regions (50).

11. Regarding claim **8**, Neilson discloses in Fig 10 the device of claim 7 wherein said individual cells forming a plurality of source regions and separating said physically isolated drain regions are packed into a relatively small area to contain at least 10 physically isolated drain regions (col 1 ln 17-20).

12. Regarding claim **9**, Neilson discloses in Fig 4 the device of claim 1 wherein said cells of said array form field effect transistors (col 1 ln 14).

13. Regarding claim **10**, Neilson discloses in Fig 10 a method for manufacturing a power semiconductor device comprising the steps of (col 3 ln 57- col 4 ln 10): forming a two-dimensional array of individual cells formed on a semiconductor substrate, each cell having source regions (46) within base regions (50) in the substrate, characterized in that the source regions of the cells of the array comprise a plurality of source region branches (46) each extending radially towards at least one source region branch of an adjacent cell (Fig 10), the source region branches of adjacent cells presenting juxtaposed ends, the base regions (50) of the cells of the array comprising a corresponding plurality of base region branches extending radially towards at least one base region branch of an adjacent cell (Fig 10), and the base region branches of adjacent cells merging together adjacent and between said juxtaposed ends to form a single and substantially uniformly doped base region surrounding said source regions of the individual cells of said array (Fig 10, col 1 ln 22-30).

14. Regarding claim **11**, Neilson discloses in Fig 10 the method of claim 10 comprising: forming said base regions extending from a first surface of said semiconductor substrate with radially extending base region branches (col 3 ln 65); forming said source region within each base region of each individual cell with said radially extending source region branches (col 4 ln4); forming a gate oxide region over said first surface (col 4 ln 5); forming a source electrode in contact with said source regions of each individual cell (c0ol 3 ln 66) within each of the plurality of the base regions; and forming a drain electrode in contact with a second surface of said semiconductor substrate opposite to said first surface.

15. Regarding claim **12**, Neilson discloses in Fig 10 the method of claim 10 comprising the steps of forming in said first surface physically isolated drain surface regions (52) surrounded by said plurality of base regions (50).

16. Regarding claim **13**, Neilson discloses in Fig 10 the method of claim 10 wherein forming said base regions (50) comprises the step of merging said base regions of each individual cell so as to form a single base region.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

19. Claim **14** is rejected under 35 U.S.C. 103(a) as being unpatentable over Neilson and Knoch (US 5,703,389).

20. Regarding claim **14**, Neilson discloses in Fig 10 the method according to claim 109 wherein forming said base regions comprises the step of making ion implants (col 3 ln 65) before forming a source electrode over said first surface (col 3 ln 66-68), however, fails to specify the ion implant is of high voltage breakdown resistance.

Knoch teaches in Fig 4 a similar cell type FET wherein the well region (36) is a base with enhanced breakdown characteristics (col 4 ln 60-61), making it suitable for high voltage applications. It would have been obvious to one of ordinary skill in the art at the time of the invention to use the teachings of Knoch in the method of Neilson in order to produce a device with an ion implant suitable for high voltage applications.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamamoto (US 5,521,410) discloses a similar structure that is

not radial. David (US 4,651,181) discloses a radial structure not utilizing merged base regions.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John C. Ingham whose telephone number is (571) 272-8793. The examiner can normally be reached on M-F, 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John C Ingham
Examiner
Art Unit 2814

jci

HOWARD WEISS
PRIMARY EXAMINER